Listing of the Claims

The following claims are presented for the Examiner's convenience in accordance with 37 C.F.R. §1.121:

1. - 7. (Previously cancelled)

8. (Previously amended) A method of producing a wafer-interposer comprising the steps of:

attaching one or more first electrical contacts to a lower surface of a substrate comprising a B-Stage adhesive material;

attaching one or more second electrical contacts to an upper surface of the substrate, the second electrical contacts having greater surface area and greater pitch than the first electrical contacts; and

creating one or more first electrical pathways passing through the substrate and connecting the first electrical contacts to the second electrical contacts.

9. (Original) The method as recited in claim 8, wherein the first and second electrical contacts are connection pads.

10. (Currently amended) A method for producing a wafer-interposer assembly comprising the steps of:

attaching one or more first electrical contacts to a lower surface of a substrate, the substrate comprising a B-Stage adhesive material;

attaching one or more second electrical contacts to an upper surface of the substrate, the second electrical contacts having greater surface area and greater pitch than the first electrical contacts;

creating one or more first electrical pathways passing through the substrate and connecting the first electrical contacts to the second electrical contacts;

depositing a conductor on one or more third electrical contacts on an upper surface of a semiconductor wafer, the semiconductor wafer including one or more semiconductor dies and the third electrical contacts being associated with the semiconductor dies;

applying a layer of no-flow underfill to the upper surface of the semiconductor wafer;

aligning the substrate with the semiconductor wafer so that ~~the deposits of the conductor on~~ the third electrical contacts correspond with the first electrical contacts on the lower surface of the substrate;

attaching the substrate to the semiconductor wafer.

11. (Original) The method as recited in claim 10 wherein the first, second and third electrical contacts are connection pads.

12. (Previously cancelled)

13. (Original) The method as recited in claim 10 further comprising the step of applying additional metalization to one or more of the third electrical contacts to redistribute them prior to the attachment of the substrate.

14. (Original) The method as recited in claim 10 further comprising the step of adding additional metalization to one or more of the third electrical contacts to improve the contact between the conductor and the third electrical contacts.

15. (Previously amended) The method as recited in claim 10 wherein the step of attaching the substrate to the semiconductor wafer comprises the steps of:

placing the semiconductor wafer on a first flat surface and holding the semiconductor wafer in place;

placing the substrate on a second flat surface and holding the substrate in place; and

bringing the first and second flat surfaces together so that the semiconductor wafer and the substrate form an adhesive bond.

16. (Original) The method as recited in claim 10 further comprising the step of singulating the substrate and semiconductor wafer assembly into one or more semiconductor die assemblies.

17. - 19. (Previously cancelled)

20. (Original) The method as recited in claim 10 wherein each conductor is a solder ball.

21. - 22. (Previously cancelled)

23. (Original) The method as recited in claim 10 further comprising the steps:

attaching the substrate and semiconductor wafer assembly to a testing apparatus; and

testing at least one of the semiconductor dies.

24. (Original) The method as recited in claim 23 wherein the step of testing the semiconductor dies further comprises performing parametric testing on at least one of the dies.

25. - 26. (Previously cancelled)

27. (Original) The method as recited in claim 23 wherein the step of testing the semiconductor dies further comprises testing the semiconductor dies simultaneously.

28. (Original) The method as recited in claim 23 further comprising the step of grading one or more performance characteristics of each semiconductor die during testing.

29. (Original) The method as recited in claim 28 further comprising the step of singulating the substrate and semiconductor wafer assembly into one or more semiconductor die assemblies.

30. (Original) The method as recited in claim 29 further comprising the step of sorting the semiconductor die assemblies based on the one or more performance characteristics.

31. (Previously amended) The method as recited in claim 29 further comprising the step of sorting the semiconductor die assemblies into conforming and nonconforming groups.

32. (Previously added) The method as recited in claim 8 further comprising the step of mounting the substrate on a semiconductor wafer including at least one semiconductor die.

33. (Previously added) The method as recited in claim 32 wherein the step of mounting the substrate on the semiconductor wafer further comprises the step of depositing a conductor on at least one third electrical contact on an upper surface of the semiconductor wafer, the at least one third electrical contact being associated with the at least one semiconductor die.

34. (Previously added) The method as recited in claim 33 further comprising the step of aligning the substrate with the semiconductor wafer so that the deposits of the conductor on the at least one third electrical contact correspond with the first electrical contacts on the lower surface of the substrate.

35. (Previously added) The method as recited in claim 32 wherein the step of mounting the substrate on the semiconductor wafer further comprises the step of applying a layer of no-flow underfill to the upper surface of the semiconductor wafer.

36. (Cancelled)

37. (Previously added) The method as recited in claim 8 further comprising the steps of:

mounting the substrate on a semiconductor wafer including at least one semiconductor die;

attaching the substrate and semiconductor wafer assembly to a testing apparatus; and

testing a portion of the at least one semiconductor die.

38. (Previously added) The method as recited in claim 37 wherein the step of testing the portion of the at least one semiconductor die further comprises performing parametric testing on at least one of the dies.

39. (Previously added) The method as recited in claim 37 wherein the step of testing the portion of the at least one semiconductor die further comprises testing the semiconductor dies simultaneously.

40. (Previously added) The method as recited in claim 37 further comprising the step of grading one or more performance characteristics of each semiconductor die during testing.